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Attorney's Docket No.: 42P17814

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Patent Application of:)	
)	
Robert Chau et al.)	Examiner: Unknown
)	
Application No.: 10/760,028)	Art Unit: Unknown
)	
Filed: January 16, 2004)	
)	
For: TRI-GATE TRANSISTOR AND)	
METHODS TO FABRICATE SAME)	

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

INFORMATION DISCLOSURE STATEMENT

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- ☐ A statement pursuant to 37 C.F.R. §1.97(e) or
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If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 11/11, 2004


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Substitution for Form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)			Complete if Known		
			Application Number	10/760,028	
			Filing Date	January 16, 2004	
			First Named Inventor:	Robert Chau	
			Art Unit	Unknown	
			Examiner Name	Unknown	
Sheet	1	of	2	Attorney Docket Number	42P17814

U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (If known)				
		US-	6,716,684 B1	4/6/2004	Krivokapic et al.	
		US-	6,680,240 B1	1/20/2004	Maszara	
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		US-				
		US-				

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Country Code ³ Number ⁴ Kind Code ⁵ (if known)				
		EP 0 623 963 A1	11/9/1994	Siemens AG		
		WO 02/43151A	5/30/2002	Hitachi ULSI Sys Co Ltd		

Examiner Signature		Date Considered	
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				Application Number	10/760,028
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				First Named Inventor:	Robert Chau
				Art Unit	Unknown
				Examiner Name	Unknown
Sheet	2	of	2	Attorney Docket Number	42P17814
NON PATENT LITERATURE DOCUMENTS					
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published			T ²
		V. Subramanian et al., "A Bulk-Si-Compatible Ultrathin-body SOI Technology for Sub-100m MOSFETS" Proceeding of the 57th Annual Device Research Conference, pp. 28-29 (1999)			
		Hisamoto et al., "A Folded-channel MOSFET for Deepsub-tenth Micron Era", 1998 IEEE International Electron Device Meeting Technical Digest, pp 1032-1034 (1998)			
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		Hisamoto, Digh et al. "FinFET- A Self-Aligned Double-Gate MOSFET Scalable to 20 nm", IEEE Transactions on Electron Devices, Vol. 47, No. 12, December 2000, pages 2320-2325			
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